

Searching PAJ

Page 1 of 2

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 63-269699

(43)Date of publication of application : 07.11.1988

(51)Int.Cl.

H04R 3/14

(21)Application number : 62-103315

(71)Applicant : PIONEER ELECTRONIC CORP

(22)Date of filing : 28.04.1987

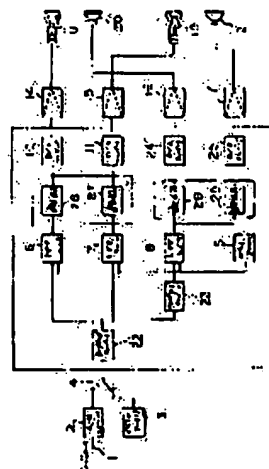
(72)Inventor : AZUMA SHUJIRO
YAMAMOTO KAORU

(54) NETWORK FOR MULTI-WAY LOUDSPEAKER DEVICE

(57)Abstract:

PURPOSE: To commonly use parts and prevent distortion in reproduced waveform, by connecting a sampling converter to the pre-stage or pre-and post-stage of a low-pass filter and connecting digital delaying circuits which correct delays in processing time produced by connected sampling filters.

CONSTITUTION: A sampling converter 23 which converts the clock frequency (f_s) of digital signals inputted through a switch 4 into a clock frequency which is lower than the clock frequency (f_s) is connected to the pre-stage of a low-pass filter 8. Then AD converters 24 and 25 which convert the digital signals into analog signals by means of low sampling signals are connected to the post-stage of the filter 8. Delaying circuits 26□29 are respectively connected to the pre- stages of the AD converters 10, 11, 24, and 25. Therefore, the scale of the hardware can be made smaller and distortion in reproduced waveform can be prevented.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

A